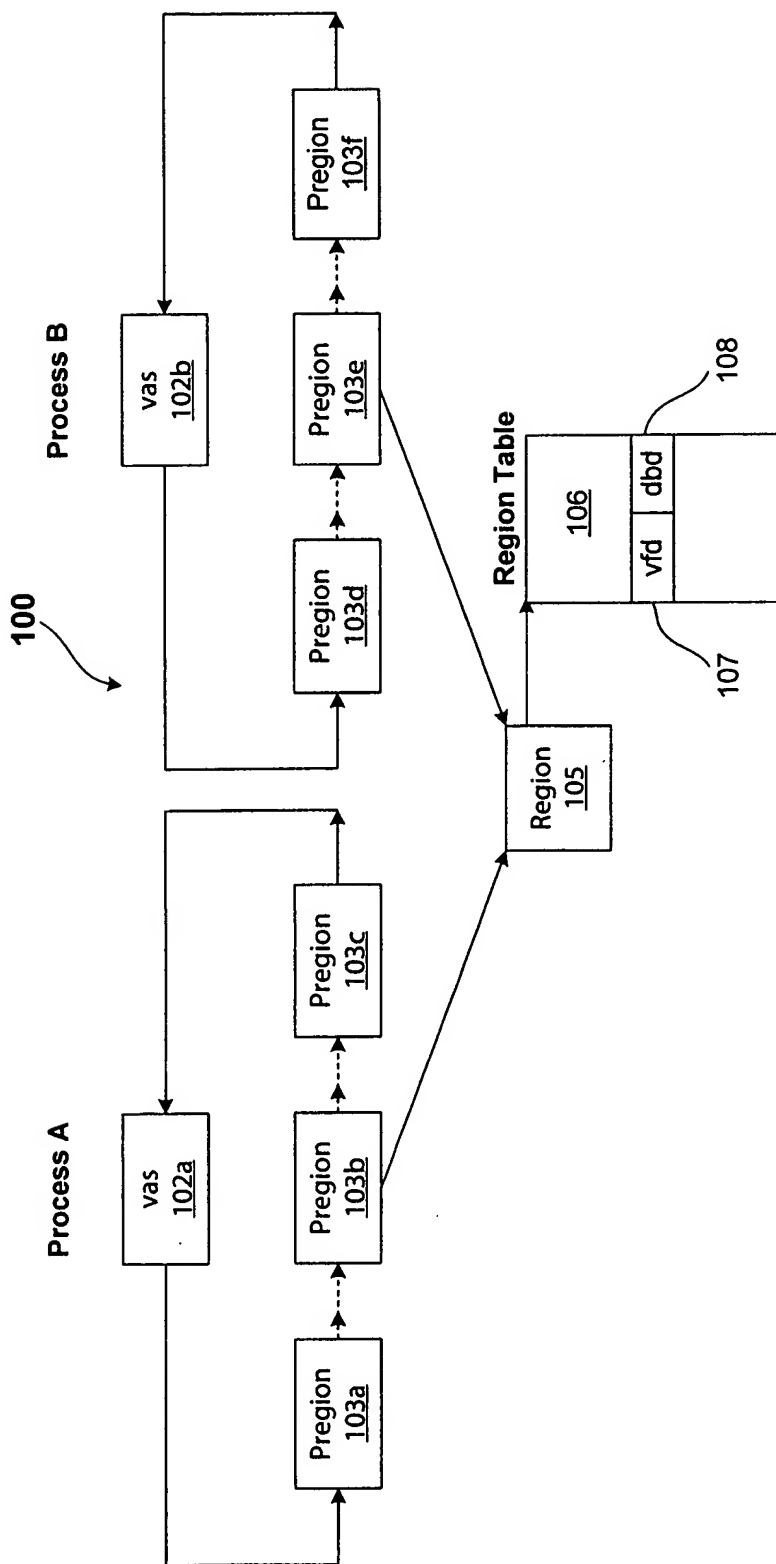




1/13



Virtual Address Space Architecture

FIG. 1

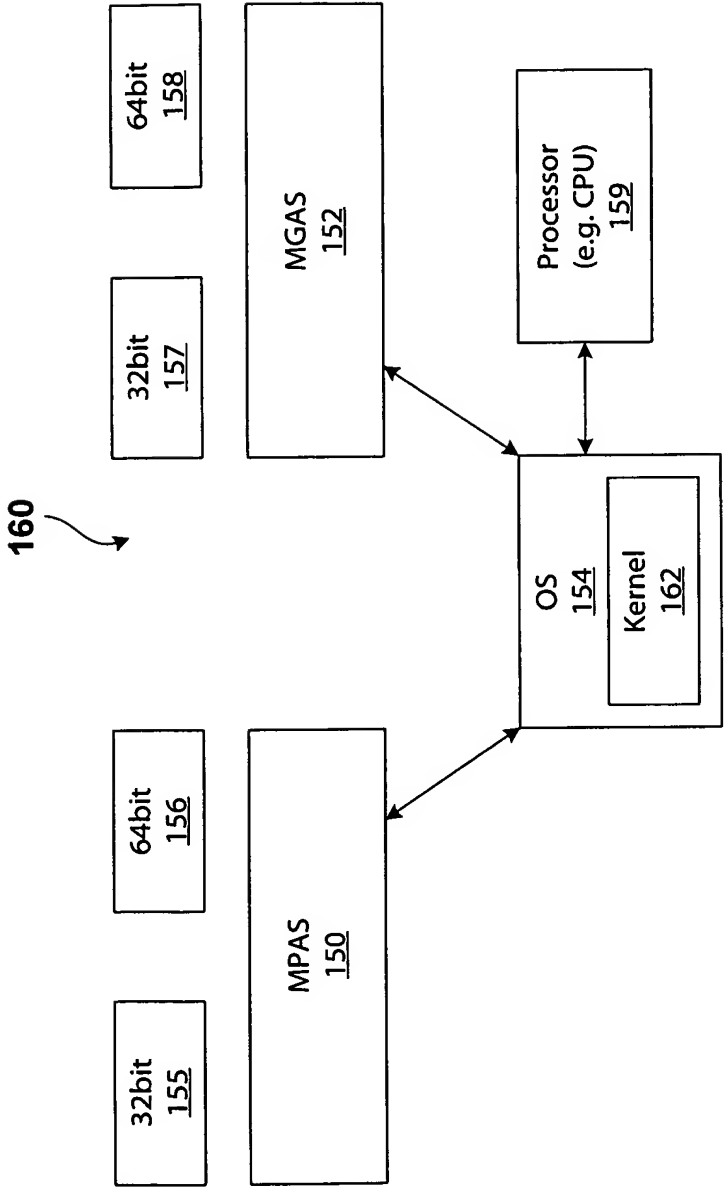


FIG. 2

3/13

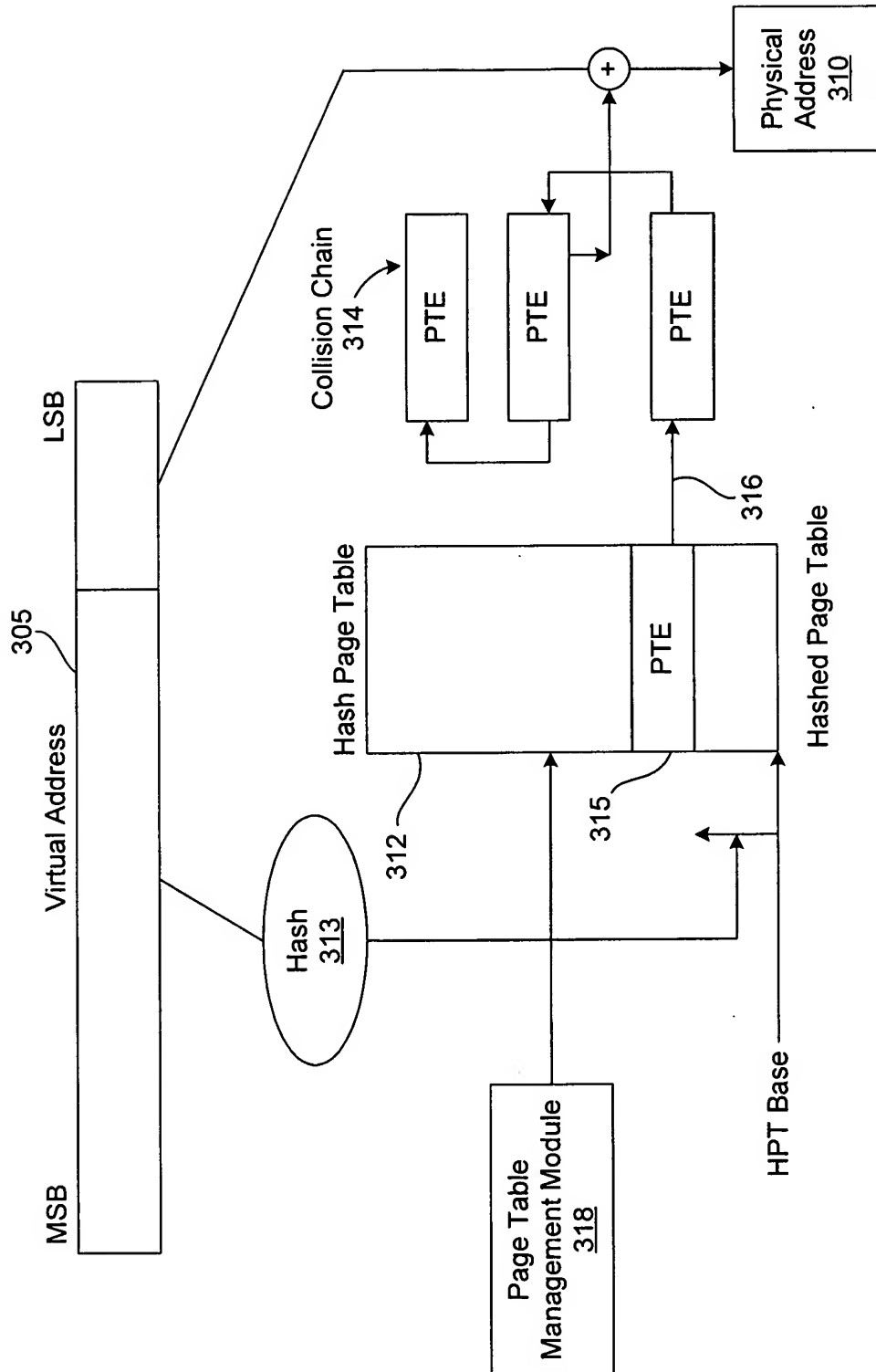
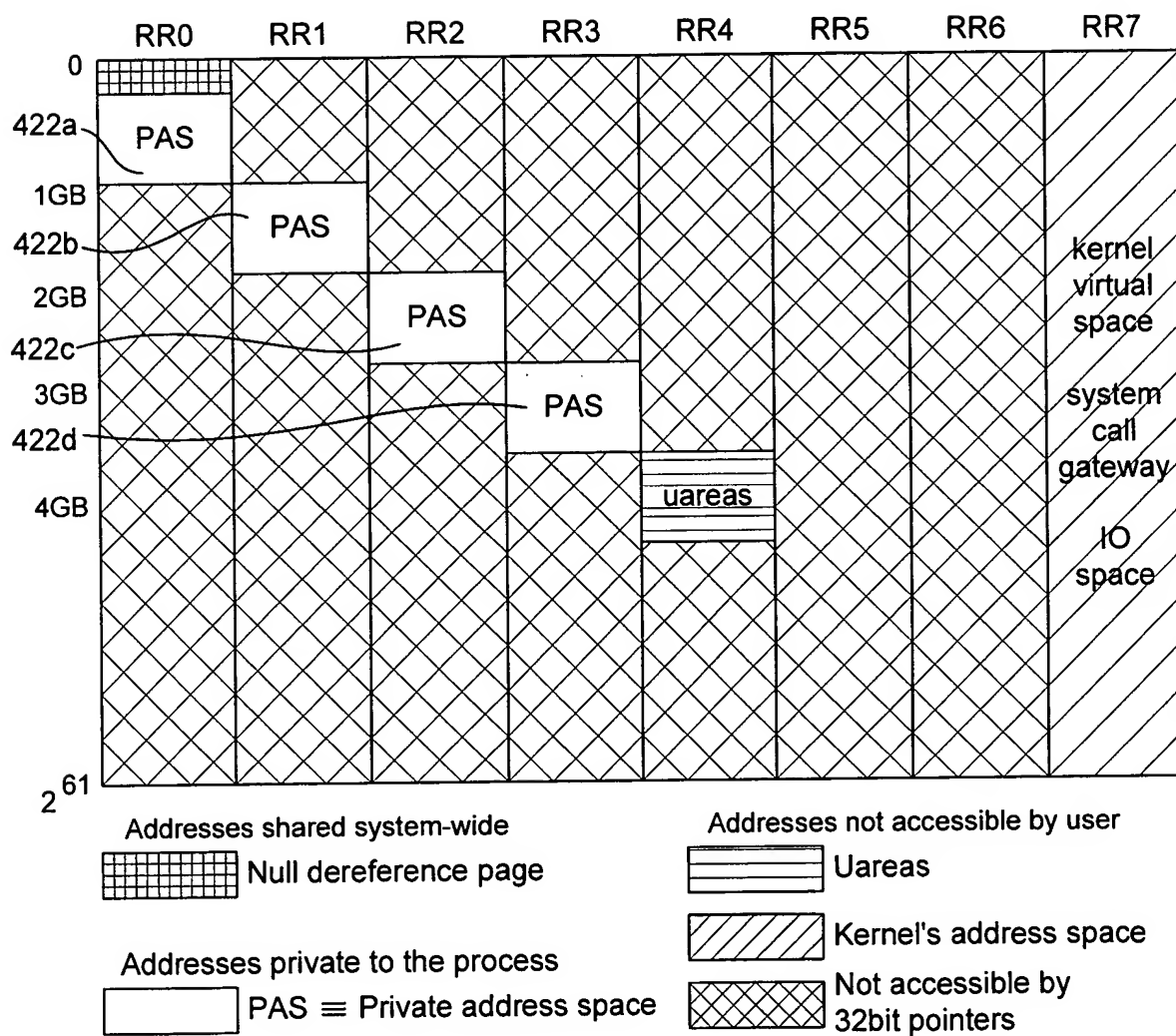


FIG. 3

4/13



32bit MPAS Address Space Layout (ASL) in segmented representation

FIG. 4A

5/13

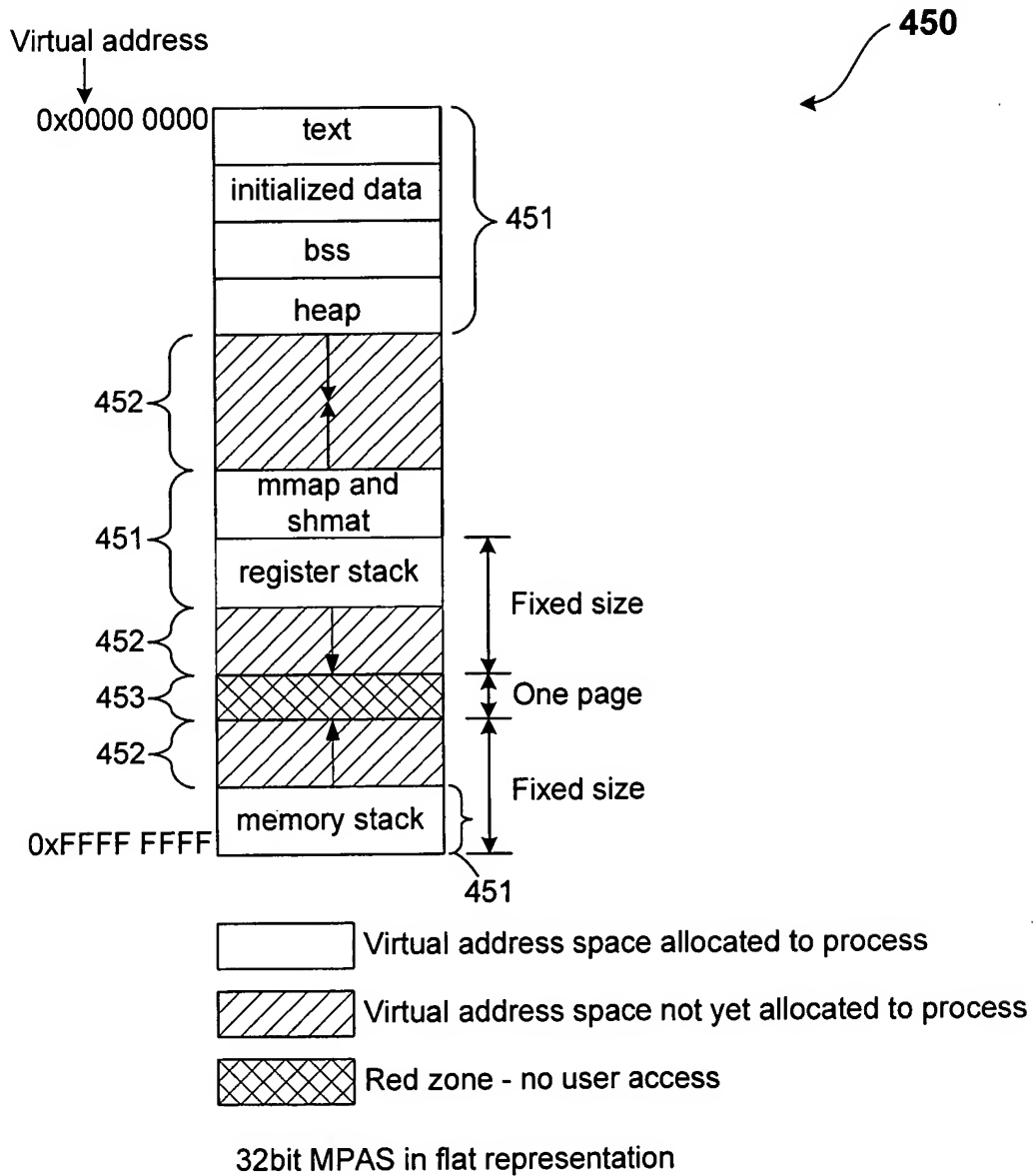
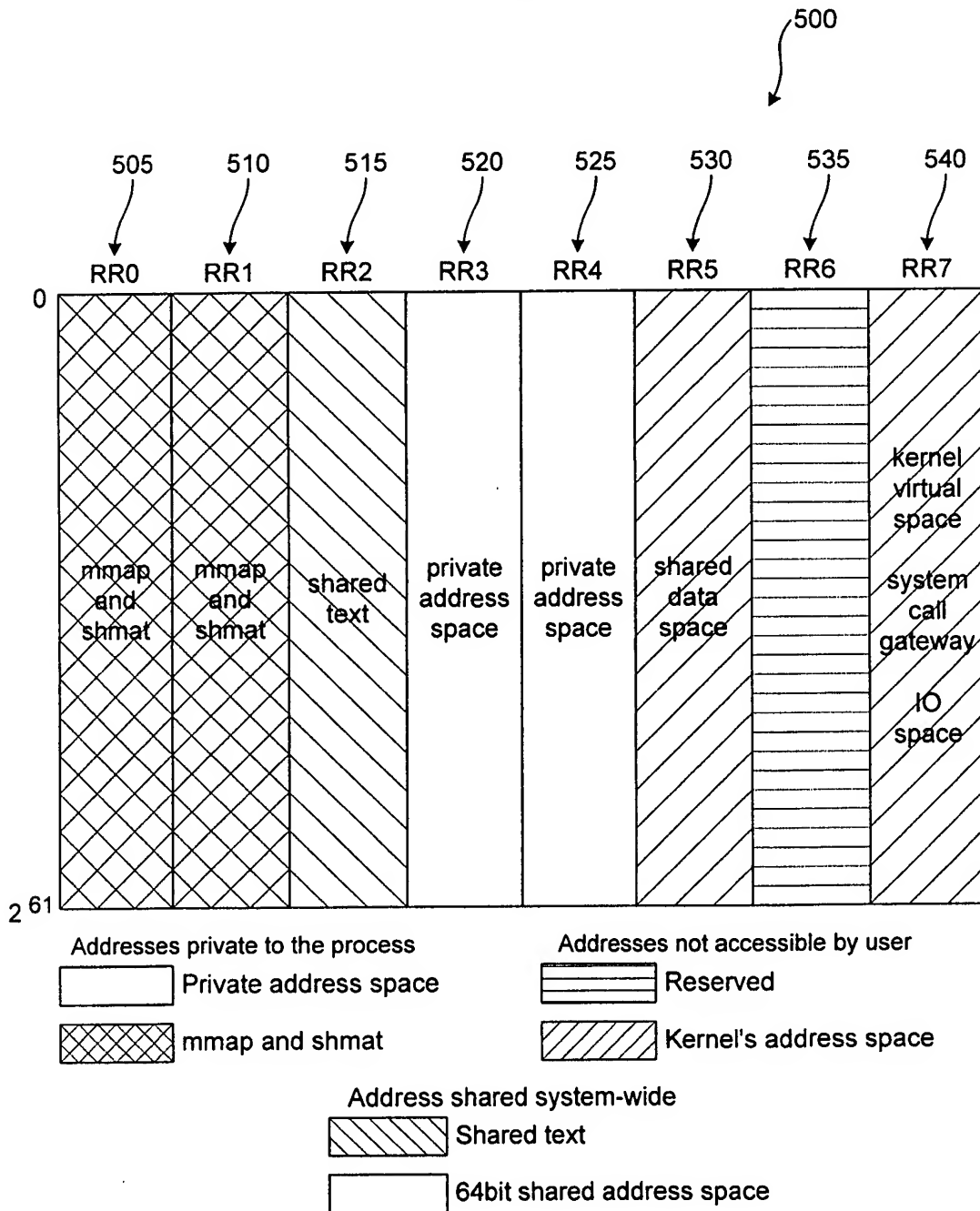


FIG. 4B

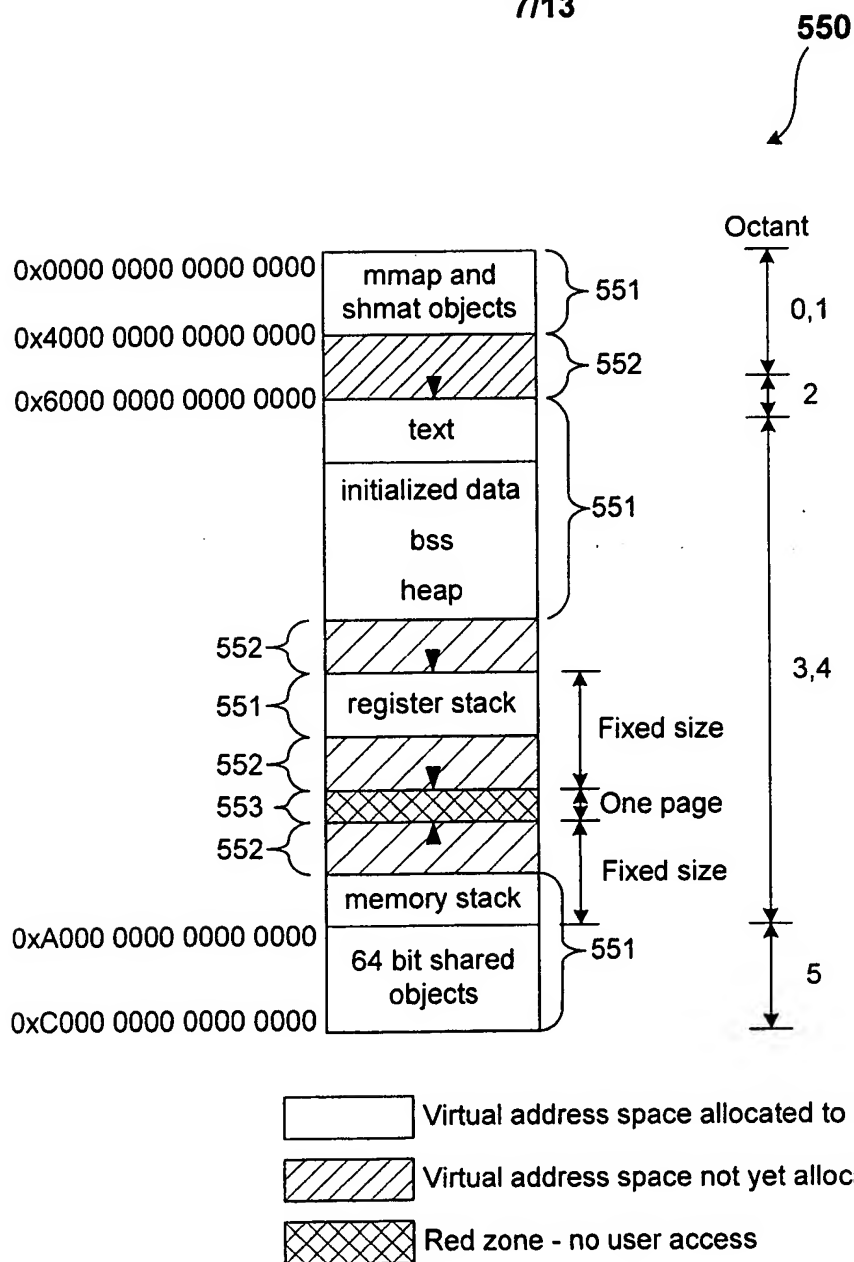
6/13



64bit MPAS (in segmented representation)

FIG. 5A

7/13



64bit MPAS in flat representation (only octants 0-5 are shown)

FIG. 5B

8/13

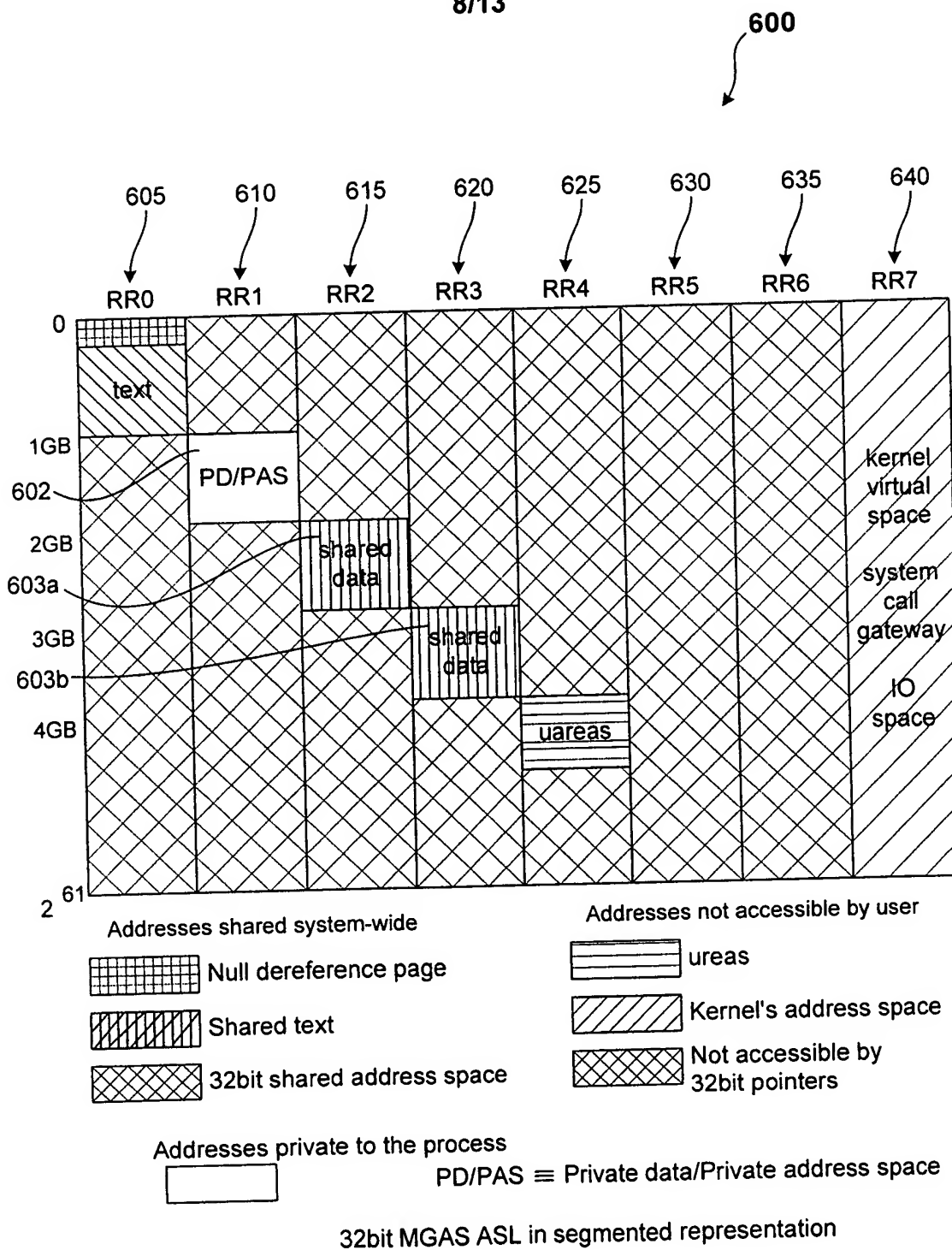
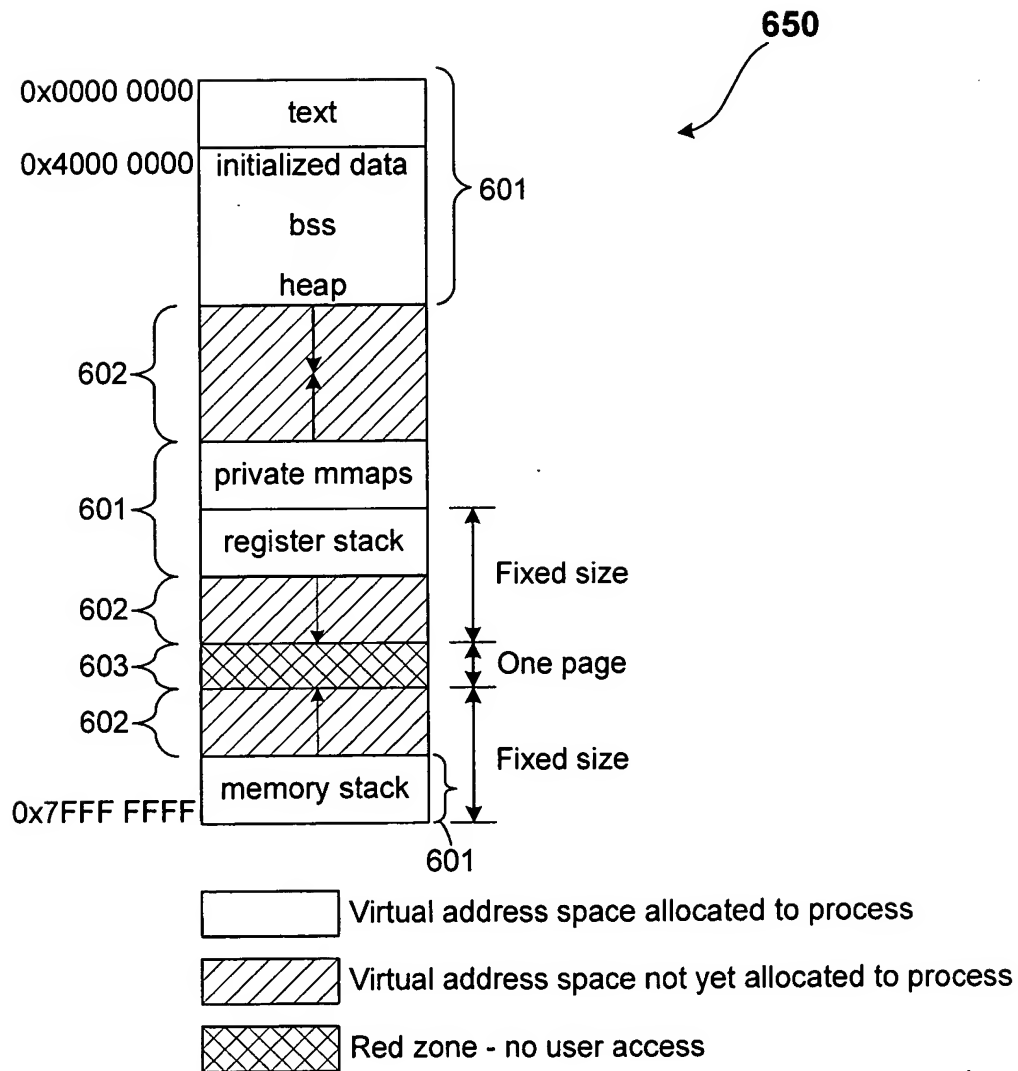


FIG. 6A

9/13



32bit MGAS ASL in flat representation

FIG. 6B

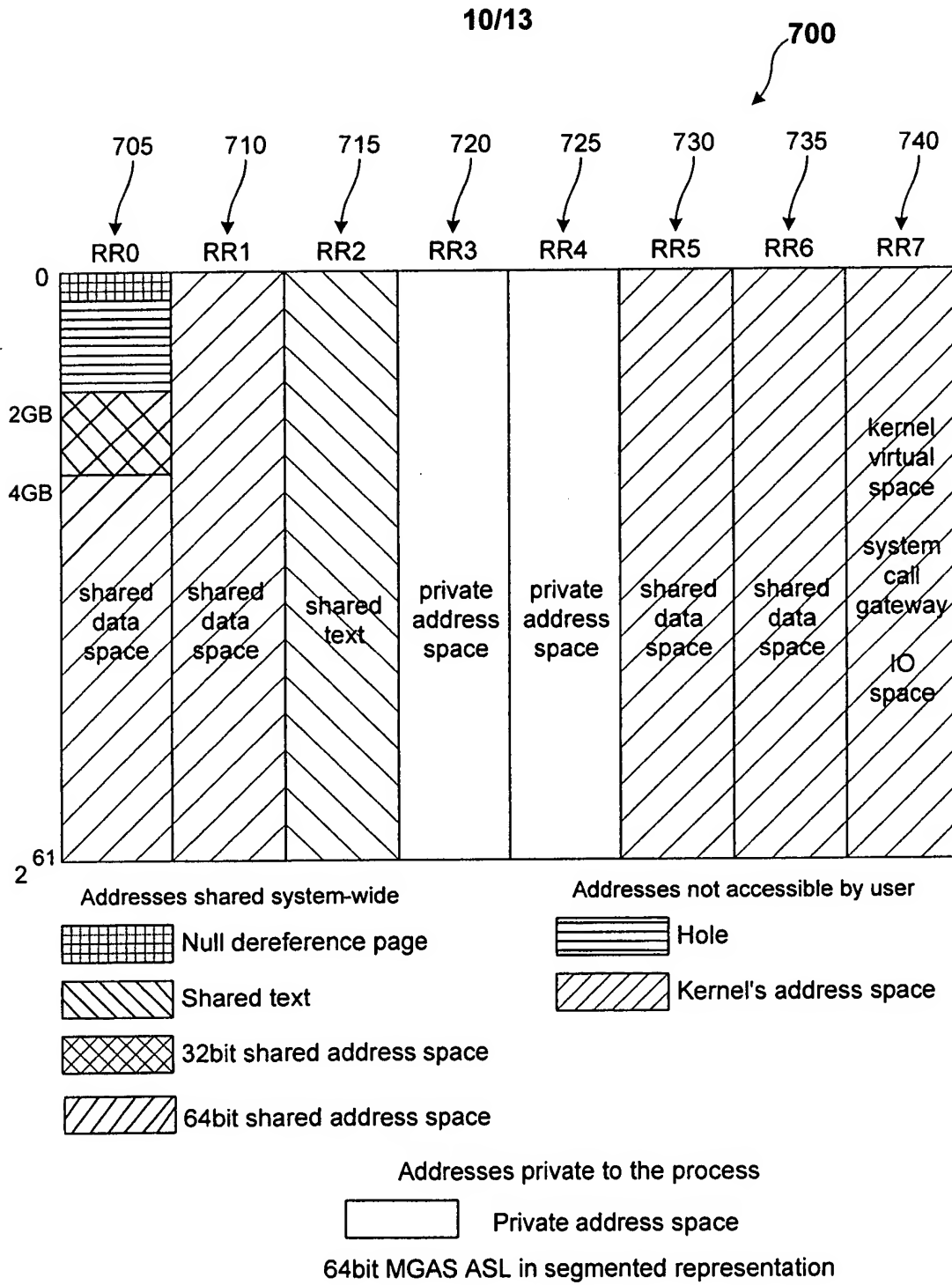
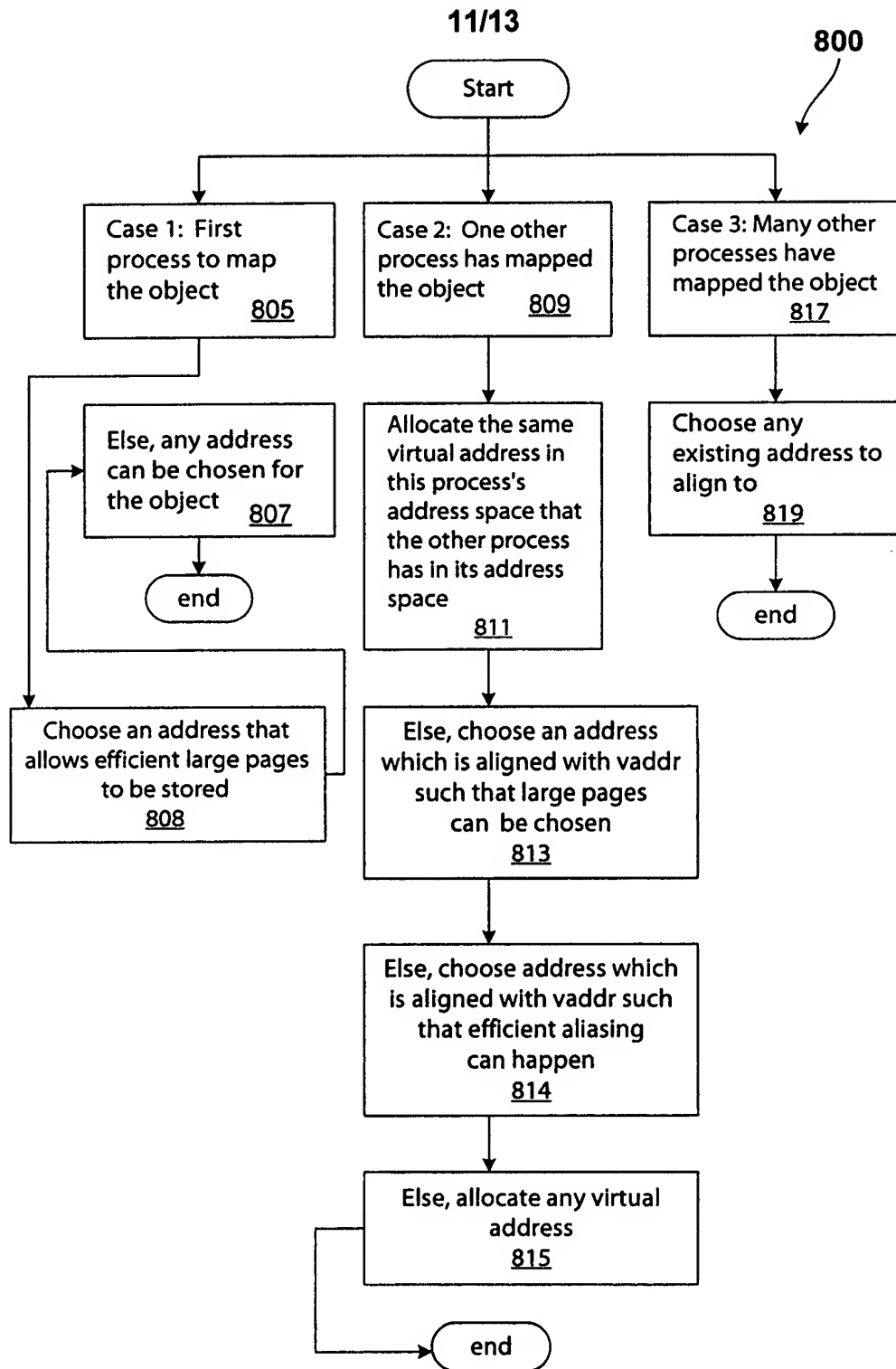


FIG. 7



Allocating Address Space for 32bit MPAS Processes

FIG. 8

12/13

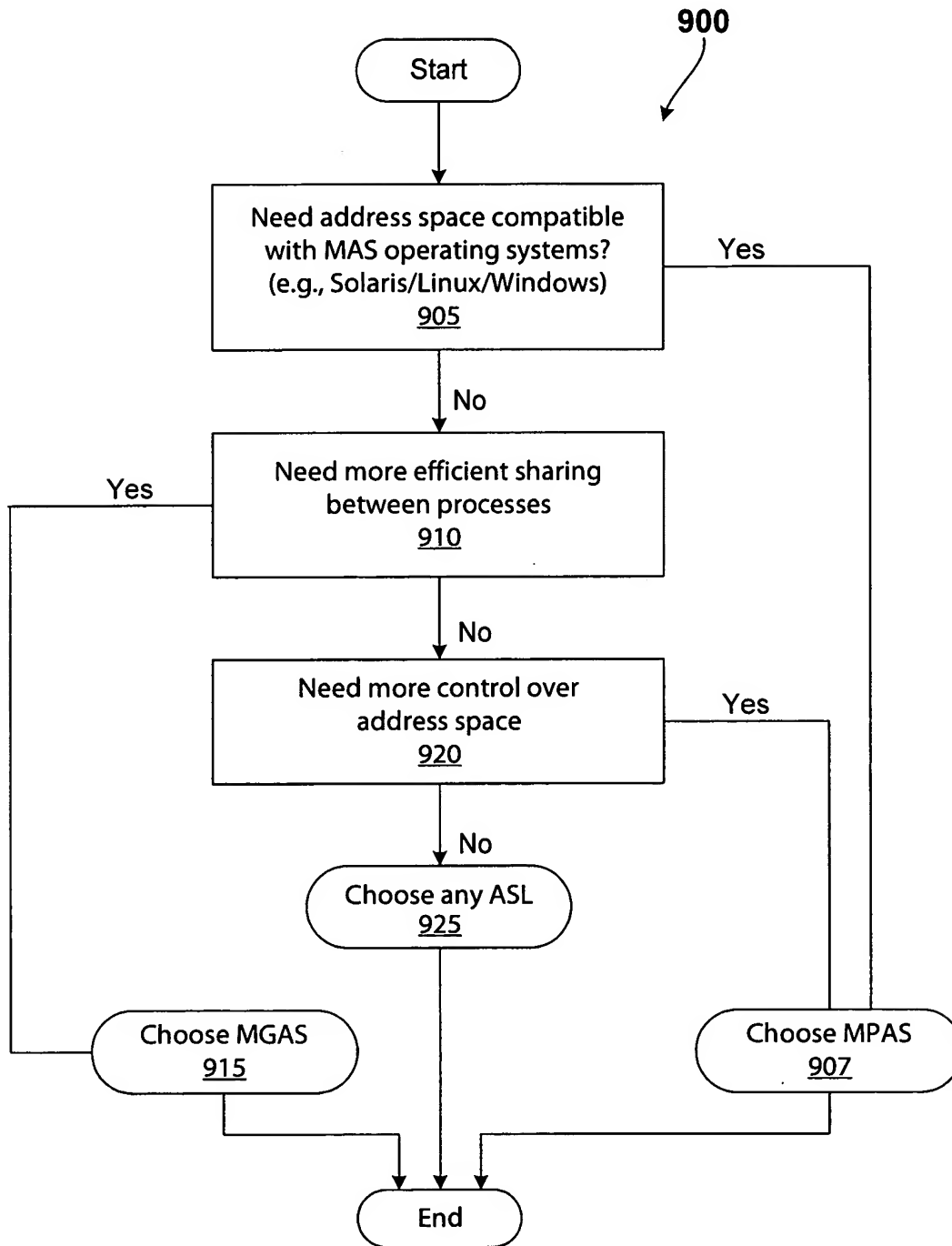


FIG. 9

13/13

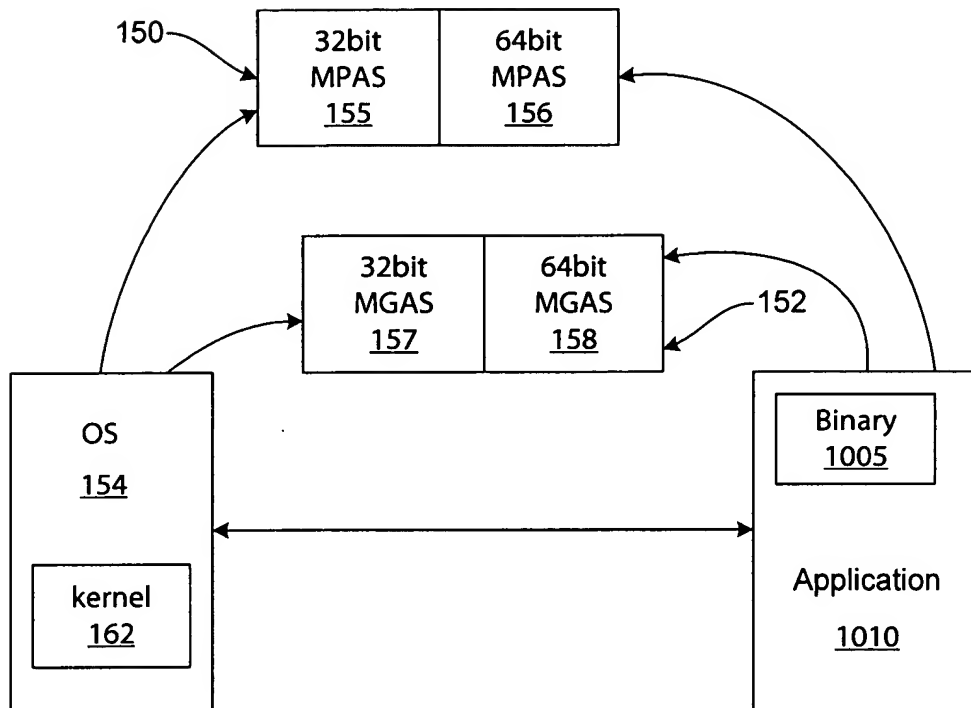


FIG. 10